

IN THE CLAIMS

1. (Amended) A peripheral bus interconnect system, comprising:

first and second peripheral bus lines that are electrically independent from one another;

first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines;

first and second controllers respectively connected to said first and second peripheral bus lines to drive said first and second bus lines in order to access and control the first and second arrays of peripheral devices connected thereto, said first and second controllers including control circuitry to send health status signals to each other to indicate the normal operation of said first and second controllers, said control circuitry being responsive to the absence of said health signals to indicate a malfunction of one of said first or second controllers; and

a normally open switch located between said first and second peripheral bus lines and adapted to be closed to connect said first and second bus lines together in response to the absence of a health status signal from a malfunctioning ~~of~~ one of said first and second controllers, whereby the first and second arrays of peripheral devices are accessed and controlled by the normally functioning other one of said first and second controllers by way of said switch,

the control circuitry of the normally functioning one of said first and second controllers generating a power down signal to shut down the malfunctioning other one of said controllers and a switch control signal to cause said normally open switch to close so that said first and second peripheral bus lines are connected together and to said normally functioning controller by way of said switch.

2. (Original) The peripheral bus interconnect system recited in claim 1, wherein each peripheral device of said first array of peripheral devices has an address which is different from the address of each of the other peripheral devices of said first array and each peripheral device of said second array of peripheral devices.

3. (Original) The peripheral bus interconnect system recited in claim 2, wherein each of said first and second controllers includes a switch control circuit, one of said first and second controllers being powered up before the other and the switch control circuit of the first to power up controller causing said normally open switch to close, whereby said first to power up controller is connected to each of said first and second peripheral bus lines by way of said switch in order to assign the different addresses to and configure the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines.

4. (Original) The peripheral bus interconnect system recited in claim 3, wherein each of said first and second controllers also includes a bus isolator, the bus isolator of the first to power up controller causing said first to power up controller to be disconnected from said first and second peripheral bus lines following the assignment of the addresses to and the configuration of the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines.

5. (Original) The peripheral bus interconnect system recited in claim 4, wherein each of said first and second controllers also includes a power control circuit, the second of said first and

second controllers being powered up by the power control circuit thereof after the first one of said controllers is powered up, such that the second to power up controller is connected to each of said first and second peripheral bus lines by way of said switch so as to access the addresses and configurations of the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines.

6. (Original) The peripheral bus interconnect system recited in claim 5, wherein the switch control circuit of the second to power up controller causes said normally open switch to open after said second to power up controller accesses the addresses and configurations of the first and second arrays of peripheral devices, whereby said first and second peripheral bus lines are disconnected from one another.

7. (Original) The peripheral bus interconnect system recited in claim 6, wherein the switch control circuit of the last to power up controller is adapted to send a health status signal to the switch control circuit of the first to power up controller to indicate that said last to power up controller is powered up and operating normally and that said normally open switch is open, the switch control circuit of said first to power up controller causing the bus isolator of said first to power up controller to be deactivated in response to the health status signal sent by said last to power up controller.

8. (Cancelled)

9. (Original) The peripheral bus interconnect system recited in claim 1, wherein each of said first and second peripheral bus lines is an electrical signal trace, said first and second arrays of peripheral devices respectively coupled to said first and second peripheral bus lines at said electrical signal traces.

10. (Original) The peripheral bus interconnect system recited in claim 9, wherein said electrical signal traces of said first and second peripheral bus lines are formed on a peripheral bus panel, said electrical signal traces being detachably connected to said normally open switch.

Please add the following newly presented claims:

11. (New) A peripheral bus interconnect system, comprising:

first and second peripheral bus lines that are electrically independent from one another;

first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines;

first and second controllers respectively connected to said first and second peripheral bus lines to drive said first and second bus lines in order to access and control the first and second arrays of peripheral devices connected thereto, each of said first and second controllers including a switch control circuit and a bus isolator; and

a normally open switch located between said first and second peripheral bus lines and adapted to be closed to connect said first and second bus lines together in response to a malfunctioning one of said first and second controllers, whereby the first and second arrays of

peripheral devices are accessed and controlled by the normally functioning other one of said first and second controllers by way of said switch,

one of said first and second controllers being powered up before the other and the switch control circuit of the first to power up controller causing said normally open switch to close temporarily, whereby said first to power up controller is connected to each of said first and second peripheral bus lines by way of said switch in order to assign addresses to and configure the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines, and

the bus isolator of the first to power up controller causing said first to power up controller to be disconnected from said first and second peripheral bus lines following the assignment of the addresses to and the configuration of the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines, whereupon the second to power up controller is connected to each of said first and second peripheral bus lines by way of said switch so as to access said first and second arrays of peripheral devices respectively connected thereto.

12. (New) The peripheral bus interconnect system recited in claim 11, wherein each of said first and second controllers also includes a power control circuit, the second of said first and second controllers being powered up by the power control circuit thereof after the first one of said controllers is powered up, such that the second to power up controller is connected to each of said first and second peripheral bus lines by way of said switch so as to access the addresses and configurations of the first and second arrays of peripheral devices respectively connected to said first and second peripheral bus lines.

13. (New) The peripheral bus interconnect system recited in claim 12, wherein the switch control circuit of the second to power up controller causes said normally open switch to open after said second to power up controller accesses the addresses and configurations of the first and second arrays of peripheral devices, whereby said first and second peripheral bus lines are disconnected from one another.

14. (New) The peripheral bus interconnect system recited in claim 13, wherein the switch control circuit of the last to power up controller is adapted to send a health status signal to the switch control circuit of the first to power up controller to indicate that said last to power up controller is powered up and operating normally and that said normally open switch is open, the switch control circuit of said first to power up controller causing the bus isolator of said first to power up controller to be deactivated in response to the health status signal sent by said last to power up controller.

15. (New) The peripheral bus interconnect system recited in claim 11, wherein each of said first and second peripheral bus lines is an electrical signal trace, said first and second arrays of peripheral devices respectively coupled to said first and second peripheral bus lines at said electrical signal traces.

16. (New) The peripheral bus interconnect system recited in claim 15, wherein said electrical signal traces of said first and second peripheral bus lines are formed on a peripheral bus panel, said electrical signal traces being detachably connected to said normally open switch.